IDEC Chip Design Contest

11-bit 10-MS/s SAR ADC with Capacitor Calibration for CDAC

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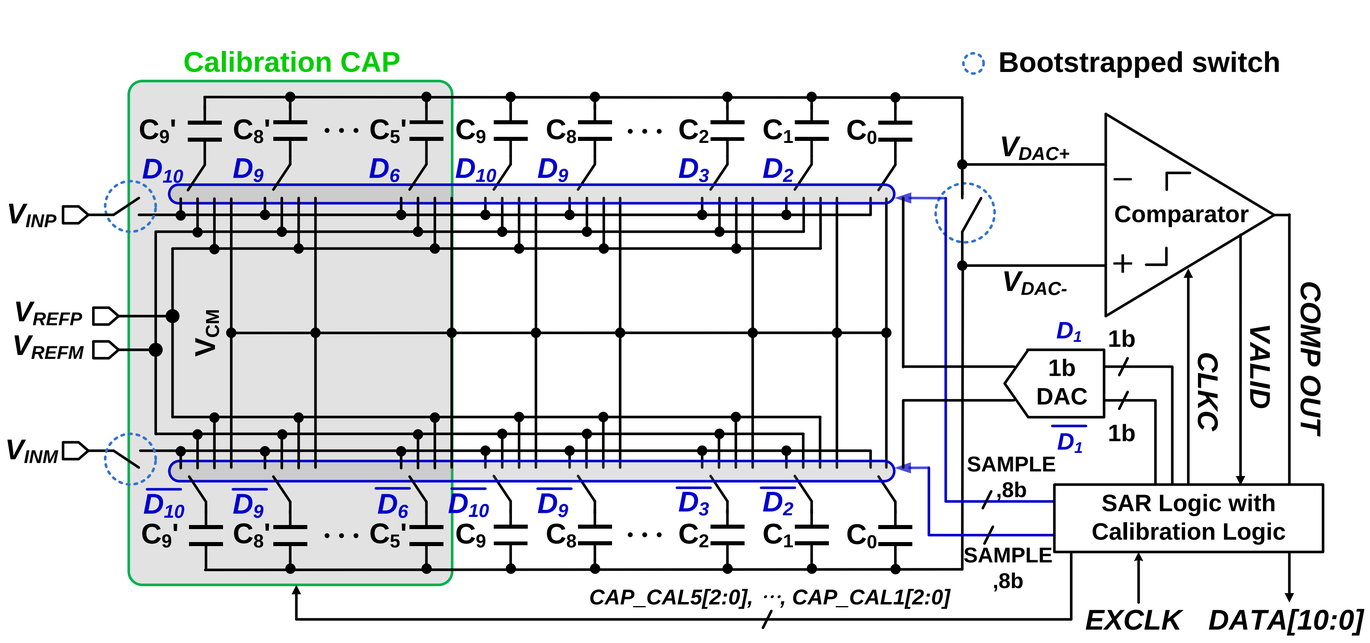
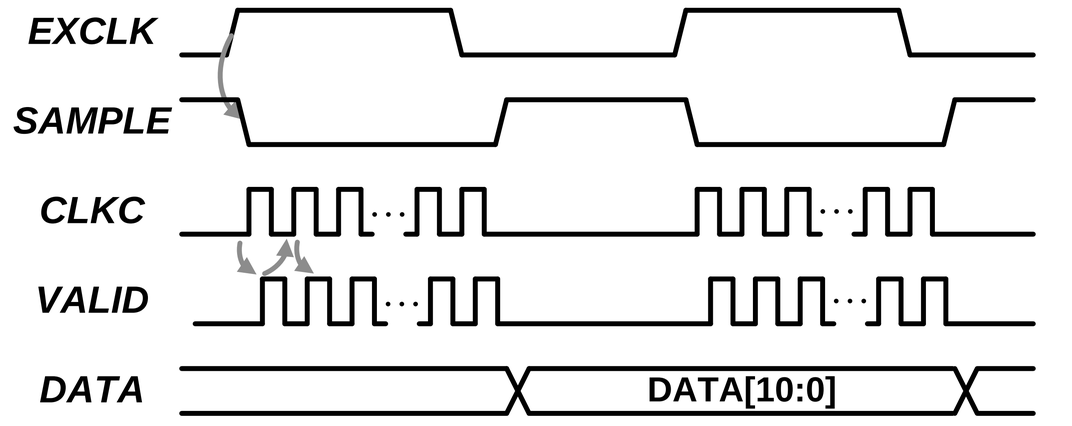
Block and Time Diagrams of Proposed SAR ADC

Block and Timing Diagrams Proposed SAR ADC

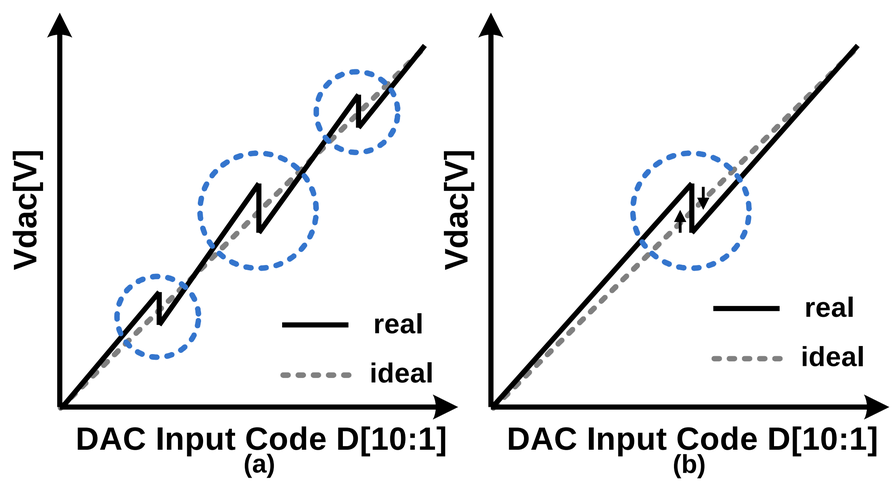




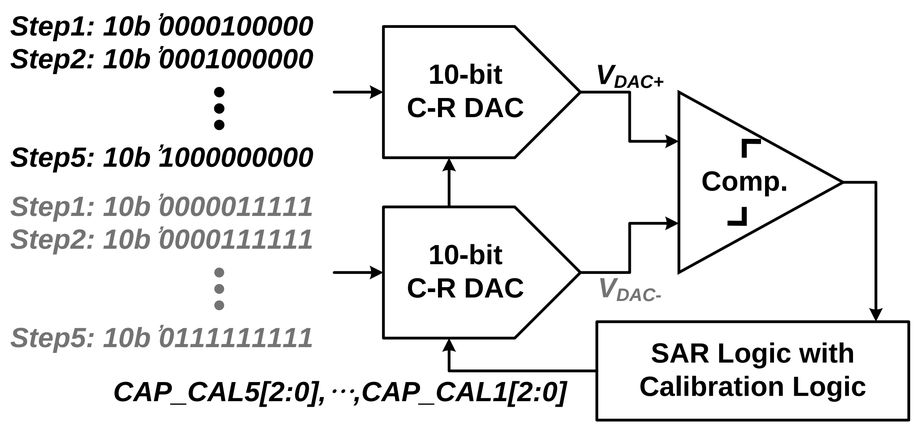
- The proposed 11-bit 10M-S/s successive approximation register (SAR) analog-to-digital converter (ADC) consists of a capacitor-resistor(C-R) digital-to-analog converter (DAC), comparator, and calibration logic.
- An asynchronous SAR architecture is used to output data conversion results per cycle of EXCLK.

Proposed Capacitor Calibration and Building Block

Capacitor Calibration



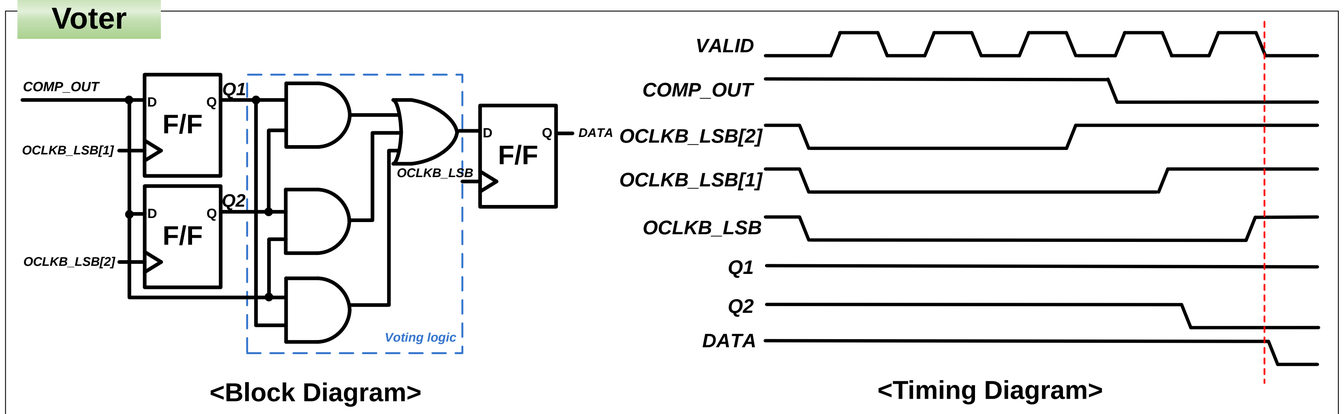
<Transfer curve of CDAC>



<Flow of calibration for upper 5-bit capacitors of CDAC>

- Capacitor Calibration
  - calibrates the upper 5-bit capacitor to compensate capacitor mismatch errors.
  - Calibration capacitors are defined as C_9', C_8', C_7', C_6' and C_5'.
  - The Capacitors of C_9', C_8', C_7', C_6' and C_5' are calibrated sequentially through Step1 to Step5, and are controlled by calibration codes from CAP_CAL5[2:0] to CAP_CAL1[2:0].

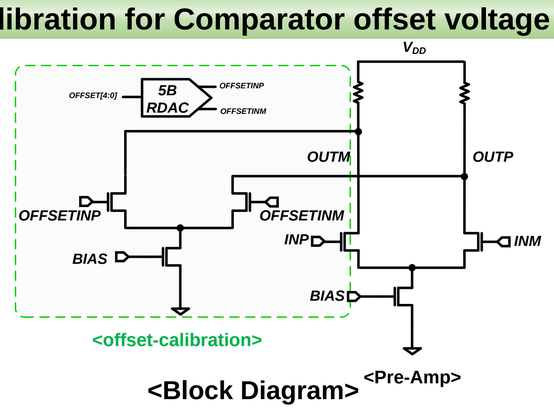
Voter



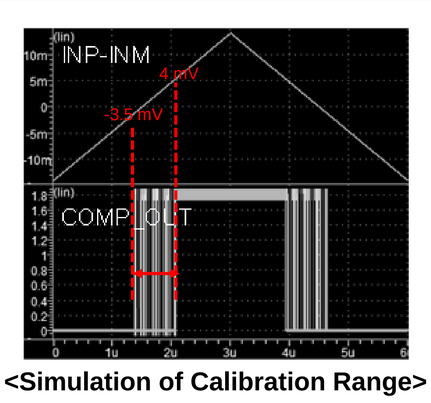
<Block Diagram> <Timing Diagram>

- In order to reduce dynamic noise during capacitor calibration, a majority voter is used to determine the final result from the result of three comparisons of the comparator for the same input.

Calibration for Comparator offset voltage



<Block Diagram> <Pre-Amp>

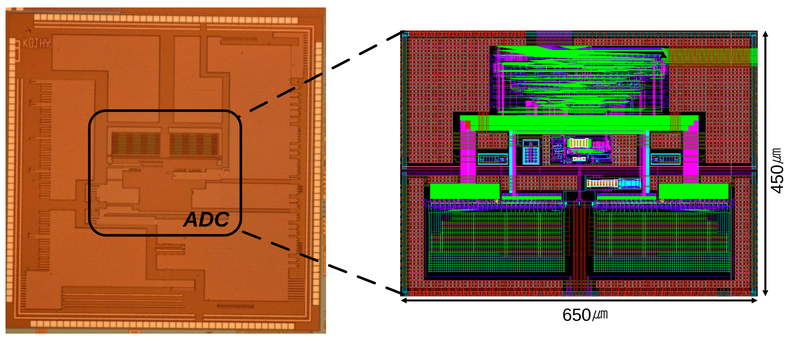


<Simulation of Calibration Range>

- The compensation of the offset voltage of the comparator is required before performing the capacitor calibration technique.
- Calibration range : -3.5 mV ~ +4mV (resolution of calibration: 0.2 mV)

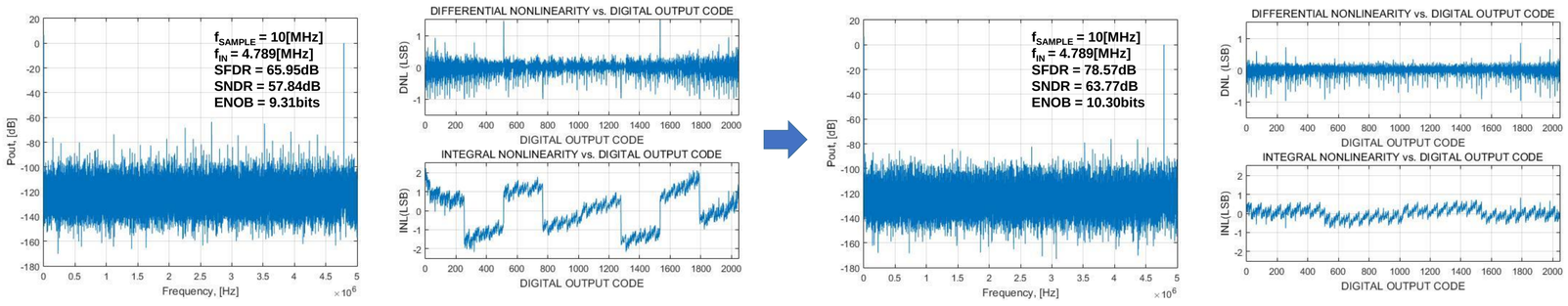
Chip Implementation and Measurement Results

Chip Implementation



- Process & Supply: 180-nm 1-poly 5-metal CMOS process w/ MIM capacitor and 1.8V supply voltage
- Power consumption: 583 ㎼
- Core area: 650 ㎛ × 450 ㎛

Measurement Results



<w/o capacitor calibration> <w/ capacitor>

- Proposed capacitor calibration used in the SAR ADC
  - improves ENOB from 9.31 bits to 10.30 bits.
  - improves DNL from -1/1.588 LSB to -0.975/0.855 LSB.
  - improves INL from -2.171/2.227 LSB to -0.798/0.832 LSB.

※ This research was conducted using the MPW program and CAD tools supported by IC Design Education Center (IDEC).

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